What is Claimed is:

[c1] A comparater comprising:

> a circult for setting a trip point of a rising edge of an input signal according to a value of an external voltage reference; and at least two transistors, in said circuit, for setting a trip point of a falling edge of said input signal according to a width-to-length ratio of said at least two transistors.

[c2] The comparator of claim 1, wherein said comparator cycles between an analog circuit and a digital circuit.

> The comparator of claim 2, wherein in said analog circuit, one of said at least two transistors is altail current source transistor, and wherein said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on.

> The comparator of claim 3, further comprising a plurality of transmission gates in said circuit, whereit said rise in said input signal causes said comparator to appear as a differential pair in an open loop configuration.

> The comparator of claim 2, wherein in said digital circuit, said input signal is at an input voltage greaten than said external reference voltage.

> The comparator of claim 15, further comprising a plurality of transmission gates in said circuit, wherein said input signal causes said comparator to appear as an asymmetric inverting Schmitt trigger.

The comparator of claim 1 wherein said at least two transistors comprises: a first transistor of length (L \downarrow) and a width of (W \downarrow); and a second transistor of length (L $_{\text{U}}$) and a width of (W $_{\text{U}}$), wherein said width-to-length ratio equals (W $_{\rm X}$ L $_{\rm Y}$)/(W $_{\rm X}$ L $_{\rm X}$), and wherein as said input signal decreases, a switching threshold becomes dependent on said width-to-length ratio.

> The comparator of claim 7, wherein said trip point of a falling edge of an input signal decreases by decreasing said width-to-length ratio.

[c4]

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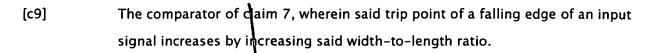
[c6]

[c5]

[c7]

[c8]

[c11]



[c10] A comparator comprising:

a circuit for setting a trip point of a rising edge of an input signal according to a value of an external voltage reference; and at least two transistors, in said circuit, for setting a trip point of a falling edge of the input signal according to a width-to-length ratio of said at least two transistors.

wherein said comparator cycles between an analog circuit and a digital circuit.

wherein said trip point of a falling edge of an input signal decreases by decreasing said width-to-length ratio, and wherein said trip point of a falling edge of an input signal increases by increasing said width-to-length ratio.

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The comparator in claim 10, wherein said at least two transistors comprises:

- a first transistor of length (L $_{\rm X}$) and a width of (W $_{\rm X}$); and a second transistor of length (L $_{\rm Y}$) and a width of (W $_{\rm Y}$), wherein said width-to-length ratio equals (W $_{\rm X}$ L $_{\rm Y}$)/(W $_{\rm Y}$ L $_{\rm X}$), and wherein as said input signal decreases, a switching threshold becomes dependent on said width-to-length ratio.
- [c12] The comparator of claim 10, wherein said analog circuit further comprises a tail current source transistor, and wherein said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on.
- [c13] The comparator of claim 12, further comprising a plurality of transmission gates in said circuit, wherein said rise in said input signal causes said comparator to appear as a differential pair in an open loop configuration.
- [c14] The comparator of claim 10, wherein in said digital circuit, said input signal is an input voltage greater than said external reference voltage.
- [c15] The comparator of claim 14, further comprising a plurality of transmission gates

in said circuit, wherein said input signal causes said comparator to appear as an asymmetric inverting Schmitt trigger.

[c16] A comparator for controlling a trip point of a rising and falling edge of an external input signal comprising a first portion operatively connected to a second portion, wherein said comparator cycles between an analog circuit and a digital circuit.

[c17] The comparator of claim 16, wherein said analog circuit comprises:

an input signal source inputting an input signal;

an output signal source;

a power supply voltage source;

an external input signal source;

a tail current source transistor operatively connected to said power supply voltage source;

a first pair of transistors operatively connected to said tail current source transistor, said input signal source, and said external input signal source; a second pair of transistors operatively connected to said first pair of transistors; and

a plurality of invertors operatively connected to said output signal source, said first pair of transistors, and said second pair of transistors.

[c18] The comparator of claim 16, wherein said digital circuit comprises:

an input signal source inputting an input signal;

an output signal source;

a power supply voltage source;

a tail current source transistor operatively connected to said power supply voltage source and said input signal source;

a first pair of transistors operatively connected to said tail current source transistor and said input signal source;

a current mirror load transistor operatively connected to said input signal source and said first pair of transistors; and

a plurality of invertors operatively connected to said output signal source, said first pair of transistors, and said current mirror load transistor.



[c19] The comparator of claim 17, wherein in said analog circuit, said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on.

[c20] The comparator of claim 18, wherein in said digital circuit, said input signal is an input voltage greater than said external reference voltage.

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